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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,391	12/04/2003	Gregory J. Hewlett	TI-34906	7532

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EXAMINER	
PERVAN, MICHAEL	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
05/13/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/727,391	HEWLETT, GREGORY J.	
	Examiner	Art Unit	
	Michael Pervan	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11-18 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-18 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed August 4, 2008 have been fully considered but they are not persuasive.

Applicant (on pages 6-7 of argument) argues that Hewlett does not disclose, teach or suggest "creating a linearity error in at least one image bit". Examiner respectfully disagrees.

The linearity error is created in Hewlett when the resets of image segments n+1 and n+2 are skewed. This error remains even though segments n and n+2 offset the error created. The counterskew mentioned by applicant only occurs when segments n and n+2 are in different bit planes. Even with this counterskew the error created still remains, it is just compensated for by the compensation periods. Therefore, Hewlett still reads on the claims and the rejection stands.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8, 11-18 and 21-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hewlett et al (US 6,008,785; submitted by applicant).

In regards to claim 1, Hewlett discloses (Figure 9b) a method of creating an image, the method comprising: operating a display to create a linearity error in at least one image bit via a sequence of bit display periods, said bit display periods comprising:

at least one conflict bit period (col. 9, lines 42; since there is a fix for conflict bits (reset conflicts), then they must exist) skewed with respect to other said bit display periods of at least one image bit (Figure 9b and col. 9, lines 53-62; as can be seen from the drawing, segments n+1 and n+2 have been skewed while segment n has not); and

at least two compensating bit periods (segments n and n+2) of at least one image bit having a bit period such that the linearity error created by said skewing occurs during said compensating bit periods and remains within the image bit (col. 9, line 63-col. 10, line 1; both compensating bit periods (segments n and n+2) have errors (increase display times) caused by the skewing).

In regards to claim 2, Hewlett discloses (Figures 9a and 9b) the method of claim 1 in which said bit period of a first of said at least two compensating bit periods is shortened (Figures 9a and 9b; as can be seen from the drawings, first compensating bit period (segment n) is shortened) and said bit period of a second of said at least two compensating bit periods is lengthened (Figures 9a and 9b; as can be seen from the drawings, second compensating bit period (segment n+2) is lengthened).

In regards to claim 3, Hewlett discloses the method of claim 1 in which said bit period of a first of said at least two compensating bit periods is lengthened (Figures 9a

and 9b; as can be seen from the drawings, first compensating bit period (segment n) is lengthened) and said bit period of a second of said at least two compensating bit periods is shortened (Figures 9a and 9b; as can be seen from the drawings, first compensating bit period (segment n+2) is shortened).

In regards to claim 4, Hewlett discloses the method of claim 1 in which a first and a second of said at least two compensating bit periods are segments of different image bits (col. 10, lines 1-3; since the compensating bits (segments n and n+2) can be of different bit-planes, they would be part of different image bits).

In regards to claim 5, Hewlett discloses the method of claim 1 in which said bit periods of a first and a second of said at least two compensating bit periods are temporally adjacent said at least one conflict bit period (Figure 9b; as can be seen from the drawing, the compensating bit periods (segments n and n+2) are temporally adjacent to the conflict bit period (segment n+1)).

In regards to claim 6, Hewlett discloses the method of claim 1 in which said bit periods of a first and a second of said at least two compensating bit periods are temporally adjacent a combination of said at least one conflict bit period and at least one other bit period (Figure 9b; as can be seen from the drawing, there could exist bit periods (segments n-1 and n+3) prior to first compensating bit period (segment n) and after second compensating bit period (segment n+2), therefore compensating bit

periods (n and n+2) would be temporally adjacent to a combination of a conflict bit period (segment n+1) and one other bit period (segments n-1 and n+3)).

In regards to claim 7, Hewlett discloses the method of claim 1 in which said bit period of a first of said at least two compensating bit periods occurs prior to said at least one conflict bit period (Figure 9b; as can be seen from the drawing, the compensating bit period (segment n) is before the conflicting bit period (segment n)) and a second of said at least two compensating bit periods occurs following said at least one conflict bit period (Figure 9b; as can be seen from the drawing, the compensating bit period (segment n+2) is after conflicting bit period (segment n+1)).

In regards to claim 8, Hewlett discloses the method of claim 7 in which said first compensating bit period corresponds to a first image bit and a second compensating bit period corresponds to a second image bit (col. 10, lines 3-5; since compensating bit periods (segments n and n+2) can be of different bit planes, then the first compensating bit period (segment n) would correspond to a first image bit and the second compensating bit period (segment n+2) would correspond to a second image bit).

In regards to claim 11, Hewlett discloses a display comprising:

an image data source (Data In) providing a plurality of image bits; and

a display device (10) comprising at least one display element (16) operable to form an image pixel corresponding to a plurality of image bits over a sequence of bit

display periods, the bit display periods comprising a linearity error in at least one image bit, said bit display periods comprising:

at least one conflict bit period (col. 9, lines 42; since there is a fix for conflict bits (reset conflicts), then they must exist) skewed with respect to other said bit display periods of at least one image bit (Figure 9b and col. 9, lines 53-62; as can be seen from the drawing, segments n+1 and n+2 have been skewed while segment n has not); and

at least two compensating bit periods (segments n and n+2) of at least one image bit having a bit period such that the linearity error created by said skewing occurs during said compensating bit periods and remains within the image bit (col. 9, line 63-col. 10, line 1; both compensating bit periods (segments n and n+2) have errors (increase display times) caused by the skewing).

In regards to claim 12, Hewlett discloses (Figures 9a and 9b) the display of claim 11 in which said bit period of a first of said at least two compensating bit periods is shortened and said bit period of a second of said at least two compensating bit periods is lengthened (Figures 9a and 9b; as can be seen from the drawings, first compensating bit period (segment n) is shortened) and said bit period of a second of said at least two compensating bit periods is lengthened (Figures 9a and 9b; as can be seen from the drawings, second compensating bit period (segment n+2) is lengthened).

In regards to claim 13, Hewlett discloses the display of claim 11 in which said bit period of a first of said at least two compensating bit periods is lengthened (Figures 9a and 9b; as can be seen from the drawings, first compensating bit period (segment n) is lengthened) and said bit period of a second of said at least two compensating bit periods is shortened (Figures 9a and 9b; as can be seen from the drawings, first compensating bit period (segment n+2) is shortened).

In regards to claim 14, Hewlett discloses the display of claim 11 in which a first and a second of said at least two compensating bit periods are segments of different image bits (col. 10, lines 1-3; since the compensating bits (segments n and n+2) can be of different bit-planes, they would be part of different image bits).

In regards to claim 15, Hewlett discloses the display of claim 11 in which said bit periods of a first and a second of said at least two compensating bit periods are temporally adjacent said at least one conflict bit period (Figure 9b; as can be seen from the drawing, the compensating bit periods (segments n and n+2) are temporally adjacent to the conflict bit period (segment n+1)).

In regards to claim 16, Hewlett discloses the display of claim 11 in which said bit periods of a first and a second of said at least two compensating bit periods are temporally adjacent a combination of said at least one conflict bit period and at least one other bit period (Figure 9b; as can be seen from the drawing, there could exist bit

periods (segments n-1 and n+3) prior to first compensating bit period (segment n) and after second compensating bit period (segment n+2), therefore compensating bit periods (n and n+2) would be temporally adjacent to a combination of a conflict bit period (segment n+1) and one other bit period (segments n-1 and n+3)).

In regards to claim 17, Hewlett discloses the display of claim 11 in which said bit period of a first of said at least two compensating bit periods occurs prior to said at least one conflict bit period (Figure 9b; as can be seen from the drawing, the compensating bit period (segment n) is before the conflicting bit period (segment n)) and a second of said at least two compensating bit periods occurs following said at least one conflict bit period (Figure 9b; as can be seen from the drawing, the compensating bit period (segment n+2) is after conflicting bit period (segment n+1)).

In regards to claim 18, Hewlett discloses the display of claim 17 in which said first compensating bit period corresponds to a first image bit and a second compensating bit period corresponds to a second image bit (col. 10, lines 3-5; since compensating bit periods (segments n and n+2) can be of different bit planes, then the first compensating bit period (segment n) would correspond to a first image bit and the second compensating bit period (segment n+2) would correspond to a second image bit).

In regards to claim 21, Hewlett discloses logic circuitry for creating an image, the logic circuitry operable when executed to:

operate a display to create a sequence of bit display periods, said bit display periods comprising:

at least one conflict bit period skewed (col. 9, lines 42; since there is a fix for conflict bits (reset conflicts), then they must exist) with respect to other said bit display periods (Figure 9b and col. 9, lines 53-62; as can be seen from the drawing, segments n+1 and n+2 have been skewed while segment n has not); and

at least two compensating bit periods (segments n and n+2) having a bit period such that an uncorrected error created by said skewing occurs during said compensating bits (col. 9, line 63-col. 10, line 1; both compensating bit periods (segments n and n+2) have errors (increase display times) caused by the skewing), the uncorrected error causing an actual weight of at least one image bit to differ from a target weight of that image bit (Figs. 9A and 9B; as can be seen from the drawings, when the resets are skewed to correct for overlap, the weights are changed from a target weight).

In regards to claim 22, Hewlett discloses the logic circuitry of Claim 21, wherein a first and a second of said at least two compensating bit periods are segments of different image bits (col. 10, lines 1-3; since the compensating bits (segments n and n+2) can be of the same bit-plane, they would be part of the same image bit).

In regards to claim 23, Hewlett discloses (Figures 9a and 9b) the logic circuitry of Claim 21, wherein said bit period of a first of said at least two compensating bit periods

is shortened (Figures 9a and 9b; as can be seen from the drawings, first compensating bit period (segment n) is shortened) and said bit period of a second of said at least two compensating bit periods is lengthened (Figures 9a and 9b; as can be seen from the drawings, second compensating bit period (segment n+2) is lengthened).

In regards to claim 24, Hewlett discloses the logic circuitry of Claim 21, wherein said bit periods of a first and a second of said at least two compensating bit periods are temporally adjacent a combination of said at least one conflict bit period and at least one other bit period (Figure 9b; as can be seen from the drawing, the compensating bit periods (segments n and n+2) are temporally adjacent to the conflict bit period (segment n+1)).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Pervan whose telephone number is (571) 272-0910. The examiner can normally be reached on Monday - Friday between 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MVP

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629

May 8, 2009